RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2812

PATENT APPLICATION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Cheol-Ju YUN		
Serial No.:	10/774,081	Examiner:	Gurley, Lynne Ann
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Confirmation No.:	7130		
For:	SEMICONDUCTOR DEVICE AND METHOD FOR FORMING SAME USING MULTI-LAYERED HARD MASK		

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AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

This paper is responsive to the Final Office Action (Paper No. 20060610) that was mailed on 22 June 2006.

Claim Amendments begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS

1. (Currently amended) A method for forming wire lines and interconnecting contacts, the method comprising;

depositing a wire line layer, wherein depositing the wire line layer comprises depositing a metal layer consisting of a metal over a plurality of buried contact pads;

depositing a multi-layered hard mask layer on the wire line layer, the multi-layered hard mask layer including at least a first hard mask layer, a second hard mask layer, and a third hard mask layer, each of the first, second, and third hard mask layers formed of different insulating materials to have an etch selectivity with respect to each other;

patterning the multi-layered hard mask layer using a photoresist pattern to produce a multi-layered hard mask;

patterning the wire line layer using the multi-layered hard mask to form ~~wire~~ bit lines;

filling gaps between the wire lines with an insulating layer; and

forming interconnecting contacts that align with the wire lines and vertically penetrate the insulating layer where the first hard mask is protected by the second hard mask.

2. (Currently amended) The method of claim 1, ~~wherein depositing the wire line layer comprises depositing a metal layer consisting of a metal over a plurality of buried contact pads, wherein patterning the wire line layer comprises patterning the metal layer to form bit lines, and~~ wherein forming the interconnecting contaets comprises forming capacitor contacts configured to electrically connect the device and capacitors to be formed over the bit lines.

3. (Original) The method of claim 1, wherein the second hard mask comprises an insulating material having an etch selectivity with respect to the insulating layer.

4. (Previously presented) A method for forming wire lines and interconnecting contacts, the method comprising:

forming a metal layer, the metal layer consisting of a metal;

forming a multi-layered hard mask on the metal layer, the multi-layered hard mask including at least a first hard mask, a second hard mask, and a third hard mask, which are formed of different insulating materials to have an etch selectivity with respect to each other;

forming wire lines by patterning the metal layer using the multi-layered hard mask;

forming an insulating layer to fill gaps between the wire lines;

forming openings to be aligned with the wire lines and vertically penetrate the insulating layer where the first hard mask disposed on the wire lines is protected by the second hard mask;

forming insulating spacers on the sidewalls of the openings;

forming a conductive layer to fill the openings; and

forming interconnecting contacts that electrically connect the wire line layer to an active region of a semiconductor substrate by filling the openings and by node-separating the conductive layer.

5. (Previously presented) The method of claim 4, wherein forming the metal layer comprises forming the metal layer over a plurality of buried contact pads, wherein forming the wire lines comprises forming bit lines, and wherein the second hard mask comprises an insulating material having an etch selectivity with respect to the insulating layer.

6. (Previously presented) A method for forming wire lines and interconnecting contacts, the method comprising:

forming a metal layer on a first insulating layer that covers a plurality of buried contact pads;

forming a multi-layered hard mask on the metal layer, the multi-layered hard mask including at least a first hard mask, a second hard mask, and a third hard mask, each of which are formed of different insulating materials to have an etch seleetivity with respect to each other;

patterning the metal layer using the third hard mask as an etch mask to form bit lines;

forming a second insulating layer on the third hard mask to fill gaps between the bit lines;

forming openings to be aligned with the bit lines and vertically penetrate the second insulating layer and the first insulating layer where the first hard mask disposed on the bit lines is protected by the second hard mask;

forming insulating spacers on the sidewalls of the openings;

forming a conductive layer to fill the openings; and

forming interconnecting contacts filling the openings by node-separating the conductive layer.

7. (Previously presented) The method of claim 6, wherein forming the metal layer comprises forming a metal layer consisting of tungsten.

8. (Previously presented) The method of claim 6, further comprising forming a barrier layer including a titanium/titanium nitride layer under the metal layer.

9. (Previously presented) The method of claim 6, wherein forming the multi-layered hard mask comprises:

sequentially forming a first hard mask layer, a second hard mask layer, and a third hard mask layer on the metal layer;

forming the third hard mask by patterning the third hard mask layer; and

patterning the second hard mask layer and the first hard mask layer by using the third hard mask as an etch mask.

10. (Original) The method of claim 6, wherein the first hard mask layer is formed to a thinner thickness than the third hard mask layer.

11. (Original) The method of claim 10, wherein the first hard mask layer is formed of silicon nitride.

12. (Original) The method of claim 10, wherein the third hard mask layer is formed of silicon oxide.

13. (Original) The method of claim 6, wherein the second hard mask layer comprises an insulating material having an etch selectivity with respect to the second insulating layer.

14. (Original) The method of claim 13, wherein the second hard mask layer is formed of one of polysilicon and titanium nitride.

15. (Original) The method of claim 6, wherein forming openings comprises:

forming a bar-type photoresist pattern on the second insulating layer to intersect the bit lines or forming a photoresist pattern on the second insulating layer to have circular exposed portions such that the openings are formed to be circular; and

selectively etching exposed portions of the second insulating layer by using the photoresist pattern as an etch mask.

16. (Original) The method of claim 6, wherein the insulating spacer is formed of silicon oxide.

17. (Original) The method of claim 6, wherein the conductive layer is formed of conductive polysilicon.

18. (Original) The method of claim 6, wherein forming interconnecting contacts comprises:

removing the second hard mask by using the first hard mask as an etch stopper; and

node-separating the conductive layer using etching.

19. (Original) The method of claim 18, wherein node-separating the conductive layer using etching comprises one chosen from the group consisting of spin processing and chemical mechanical polishing.

20. (Original) The method of claim 6, wherein the interconnecting contacts are capacitor contacts configured to be electrically connected to capacitors formed over the bit lines.

21-25. (Cancelled)